WHAT IS CLAIMED IS:

1. A semiconductor device having a transistor with a gate, a source, and a drain formed in an element active region demarcated by non-LOCOS insulating device isolation blocks on a semiconductor substrate, comprising:

at least two gates covered with insulating films and formed on said element active region to extend over said non-LOCOS insulating device isolation blocks, and

a leading-out electrode filled between adjacent ones of said gates with said insulating films intervened,

wherein upper surfaces of said gates are planarized at substantially the same level over said non-LOCOS insulating device isolation blocks and said element active region, and upper surfaces of said insulating films and an upper surface of said leading-out electrode are planarized at substantially the same level.

2. A device according to claim 1, wherein said upper surfaces of said gates, said upper surfaces of said insulating films, and said upper surface of said leading-out electrode are planarized by chemical mechanical polishing.

3. A device according to claim 1, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure which has a shield plate electrode patterned with intermediary of a shield gate insulating film and a cap insulating film covering said shield plate electrode and fixes a portion of said semiconductor substrate positioned below said shield plate electrode to a predetermined potential.

4. A device according to claim 1, wherein said non-

LOCOS insulating device isolation block is a trench type element isolation structure.

5. A semiconductor device, comprising:

a first step structure portion formed at a predetermined level from a surface of a reference layer;

second step structure portions respectively formed on said first step structure portion and said reference layer and functioning as non-LOCOS insulating device isolation blocks for demarcating an element active region on said reference layer; and

a first conductive film patterned on said element active region across at least said second step structure portion on said reference layer,

wherein an upper surface of said first conductive film is planarized such that said upper surface of said first conductive film and an upper surface of said second step structure portion formed on said first step structure portion are formed at substantially the same level.

6. A device according to claim 5, wherein said upper surface of said first conductive film and said upper surfaces of said second step structure portions are planarized by chemical mechanical polishing.

7. A device according to claim 5, wherein said reference layer is a semiconductor substrate.

8. A device according to claim 5, wherein said first step structure portion is a first insulating film formed on a scribing line region of said semiconductor substrate.

9. A device according to claim 5, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a shield plate electrode

buried in an insulating layer.

10. A device according to claim 5, wherein said first conductive film is formed of a polysilicon film, and a silicide layer of a refractory metal is formed on said first conductive film.

11. A device according to claim 5, wherein said first conductive film is a gate electrode.

12. A device according to claim 5, wherein said reference layer is a semiconductor substrate in which a groove portion is formed, a portion of said semiconductor substrate surrounding the groove portion serves as said first step structure portion, and an element region is formed in the groove portion.

13. A device according to claim 12, wherein said first step structure portion is an insulating film formed on a scribing line region of said semiconductor substrate.

14. A device according to claim 12, wherein said second step structure portion is a non-LOCOS insulating device isolation block for demarcating said element active region on an element region.

15. A device according to claim 14, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a shield plate electrode buried in an insulating layer.

16. A device according to claim 12, wherein said first conductive film is formed of a polysilicon film, and a silicide layer of a refractory metal is formed on said first conductive film.

17. A device according to claim 12, wherein said first conductive film is a gate electrode.

18. A device according to claim 5, wherein said reference layer is an insulating interlayer stacked on said semiconductor substrate, first wiring layers are formed in said first and second step structure portions, and said first conductive film functions as a second wiring layer.

19. A device according to claim 18, further comprising another insulating interlayer having a contact hole and formed under said insulating interlayer, and a memory capacitor patterned on said another insulating interlayer, in which a storage node electrode, a dielectric film, and a cell plate electrode having planarized surfaces are sequentially stacked.

20. A device according to claim 5, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

21. A semiconductor device comprising:

partially formed step structures;

at least two first conductive films patterned on a step structure nonformation region and bestriding over said step structures;

first insulating films covering said first conductive films; and

a second conductive film filling between adjacent ones of said first conductive films with said first insulating films intervened,

wherein upper surfaces of said first conductive films are planarized at substantially the same level over said step structures and said step structure nonformation region, and upper surfaces of said first insulating films and an upper surface of said second conductive film are planarized

at substantially the same level.

22. A device according to claim 21, wherein said upper surfaces of said first conductive film, said upper surfaces of said upper surfaces, and said upper surface of said second conductive film are planarized by chemical mechanical polishing.

23. A device according to claim 21, wherein said upper surfaces of said first conductive films are flush with each other.

24. A device according to claim 21, wherein said step structures are non-LOCOS insulating device isolation blocks, said step structure nonformation region is an element active region demarcated by said non-LOCOS insulating device isolation blocks, and said first conductive films are patterned on said element active region through second insulating films.

25. A device according to claim 21, wherein said first conductive film is a gate electrode, and a pair of impurity diffusion layers are formed in said element active region on both sides of said first conductive film.

26. A device according to claim 25, wherein said second conductive film is a leading-out electrode connected to one of said impurity diffusion layers.

27. A device according to claim 21, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a third conductive film patterned on a third insulating film, and a fourth insulating film covering said third conductive film.

28. A semiconductor device comprising:

non-LOCOS insulating device isolation blocks for

demarcating an element formation region on a semiconductor substrate, said non-LOCOS insulating device isolation block being formed by burying a first conductive film in a first insulating film;

second conductive films filled, with intermediary of second insulating films, between adjacent ones of said non-LOCOS insulating device isolation blocks on said semiconductor substrate, capacitively coupled to said first conductive film through a side surface portion of said first insulating film, and separated into an island shape in said element formation region; and

a third conductive film patterned into a strip shape on said second conductive film through a third insulating film and capacitively coupled to said second conductive film.

29. A device according to claim 28, wherein said non-LOCOS insulating device isolation blocks are patterned into a strip shape, and said third conductive film is formed to be substantially perpendicular to said non-LOCOS insulating device isolation blocks.

30. A device according to claim 28, wherein an upper surface of said second conductive film is substantially flush with upper surfaces of said non-LOCOS insulating device isolation blocks.

31. A device according to claim 28, wherein said device comprises

a pair of impurity diffusion layers formed in surface regions of said semiconductor substrate on both sides of said second conductive film in said element formation region, and

a fourth conductive film patterned into a strip shape

to be substantially perpendicular to said third conductive film; and

one of said impurity diffusion layers is electrically connected to said fourth conductive film.

32. A device according to claim 28, wherein said third conductive film is formed of a polysilicon film, and a silicide layer of a refractory metal is formed on said third conductive film.

33. A device according to claim 28, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

34. A semiconductor device comprising:

non-LOCOS insulating device isolation blocks for demarcating an element formation region on a semiconductor substrate, said non-LOCOS insulating device isolation block being formed by burying a first conductive film in a first insulating film;

a second conductive film filled, with intermediary of second insulating films, between adjacent ones of said non-LOCOS insulating device isolation blocks on said semiconductor substrate, and capacitively coupled to said first conductive film through a side surface portion of said first insulating film.

35. A device according to claim 34, wherein said second conductive film is a floating gate separated into an island shape in said element formation region.

36. A device according to claim 34, further comprising a third conductive film patterned into a strip shape on said second conductive film with intermediary of a third insulating film and capacitively coupled to said second

conductive film.

37. A device according to claim 34, wherein said non-LOCOS insulating device isolation blocks are patterned into a strip shape, and said third conductive film is formed to be substantially perpendicular to said non-LOCOS insulating device isolation blocks.

38. A device according to claim 34, wherein an upper surface of said second conductive film is substantially flush with upper surfaces of said non-LOCOS insulating device isolation blocks.

39. A device according to claim 34, wherein said device comprises

a pair of impurity diffusion layers formed in surface regions of said semiconductor substrate on both sides of said second conductive film in said element formation region, and

a fourth conductive film patterned into a strip shape to be substantially perpendicular to said third conductive film; and

one of said impurity diffusion layers is electrically connected to said fourth conductive film.

40. A device according to claim 34, wherein said third conductive film is formed of a polysilicon film, and a silicide layer of a refractory metal is formed on said third conductive film.

41. A device according to claim 34, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

42. A semiconductor device comprising:

a semiconductor region where a pair of first diffusion

layers of a predetermined conductivity type are formed on surface regions;

a first layer having a conductive film patterned on said semiconductor region with a first insulating film intervened, said first diffusion layers being formed on left and right sides of said conductive film, a second insulating film formed on an upper surface of said conductive film, a third insulating film covering side surfaces of said conductive film and said second insulating film and planarized such that an upper surface of said third insulating film and an upper surface of said second insulating film are formed on substantially the same plane; and

a second layer patterned on said third insulating film including said upper surface of said second insulating film, in which a pair of second diffusion layers of a predetermined conductivity type are formed in regions on both sides of said second insulating film such that a region between said second diffusion layers opposes said conductive film through said second insulating film.

43. A device according to claim 42, wherein said third insulating film is planarized by chemical mechanical polishing.

44. A device according to claim 42, wherein said semiconductor region is a region on a semiconductor substrate.

45. A device according to claim 42, wherein said first and second diffusion layers are of conductivity types different from each other.

46. A device according to claim 42, wherein said first

and second diffusion layers have the same conductivity type.

47. A device according to claim 42, further comprising a step structure on said semiconductor region, said step structure being formed in said third insulating film and planarized such that an upper surface of said step structure and said upper surface of said third insulating film are on substantially the same plane.

48. A device according to claim 42, wherein a step structure is formed on said semiconductor region, and an upper portion of another conductive film having said second insulating film on an upper surface is patterned on said step structure, and

said step structure and said another conductive film are formed in said third insulating film and planarized such that said upper surface of said second insulating film and said upper surface of said third insulating film are on substantially the same plane.

49. A device according to claim 48, wherein said upper surface of said third insulating film is planarized by chemical mechanical polishing.

50. A device according to claim 48, wherein said step structure is a non-LOCOS insulating device isolation block for demarcating an element formation region as a conductive film formation portion on said semiconductor region.

51. A device according to claim 42, further comprising a silicide film consisting of a refractory metal on a surface of said first insulating film.

52. A semiconductor device having first and second transistors which have a common gate,

wherein said first transistor comprises said gate

patterned on a semiconductor substrate with intermediary of a first gate insulating film, and first source and drain formed in surface regions of said semiconductor substrate on both sides of said gate,

said second transistor comprises said gate, and second source and drain formed, on both sides of said gate, on a conductive film patterned on said gate with intermediary of a second gate insulating film formed on an upper surface of said gate, and

an insulating interlayer is formed to cover side surfaces of said gate and said second gate insulating film and planarized such that an upper surface of said insulating interlayer and said upper surface of said second gate insulating film are on substantially the same plane, said conductive film being formed on said insulating interlayer including the upper surface of said second gate insulating film.

53. A device according to claim 52, wherein said upper surface of said insulating interlayer is planarized by chemical mechanical polishing.

54. A device according to claim 52, wherein said first source and said first drain have a conductivity type different from that of said second source and said second drain.

55. A device according to claim 52, wherein said first source and said first drain have the same conductivity type as that of said second source and said second drain.

56. A device according to claim 52, wherein said conductive film is formed of a silicon film.

57. A device according to claim 52, further comprising

a silicide layer of a refractory metal formed on a surface of said gate.

58. A device according to claim 52, further comprising a step structure formed on said semiconductor substrate, said step structure being formed in said insulating interlayer and planarized such that an upper surface of said step structure and an upper surface of said insulating interlayer are on substantially the same plane.

59. A device according to claim 58, wherein said upper surface of said insulating interlayer is planarized by chemical mechanical polishing.

60. A device according to claim 52, wherein a step structure is formed on said semiconductor substrate, and an upper portion of another gate having said second gate insulating film is patterned on an upper surface of said step structure, and

said step structure and said another gate are formed in said insulating interlayer and planarized such that said upper surface of said second gate insulating film and said upper surface of said insulating interlayer are on substantially the same plane.

61. A device according to claim 60, wherein said upper surface of said insulating interlayer is planarized by chemical mechanical polishing.

62. A device according to claim 60, wherein said step structure is a non-LOCOS insulating device isolation block for demarcating an element active region where said first transistor is formed on said semiconductor substrate.

63. A semiconductor device comprising:

a first insulating film filled in a groove formed in a

semiconductor substrate;

first conductive films patterned, with intermediary of a second insulating film, on at least a first insulating film nonformation region of said semiconductor substrate over said first insulating film nonformation region and said first insulating film;

a third insulating film covering said first conductive film;

a pair of diffusion layers formed in surface regions of said semiconductor substrate on both sides of said first conductive film; and

a second conductive film filled, with intermediary of said third insulating film, between adjacent ones of said first conductive films and connected to said diffusion layer,

wherein upper surfaces of said first conductive films are planarized across said nonformation region and said first insulating film on substantially the same plane, and an upper surface of said third insulating film and an upper surface of said second conductive film are planarized on substantially the same plane.

64. A device according to claim 63, wherein said upper surfaces of said first conductive films and said second conductive film are planarized by chemical mechanical polishing.

65. A device according to claim 63, wherein said first and second conductive films are formed of silicon films.

66. A device according to claim 63, wherein said first insulating film filled in the groove is a non-LOCOS insulating device isolation block for demarcating an element

active region on said semiconductor substrate.

67. A device according to claim 63, further comprising a diffusion prevention film covering at least an inner wall surface of the groove, and wherein said first insulating film is filled in the groove with intermediary of said diffusion prevention film.

68. A semiconductor device in which a transistor having a gate, a source, and a drain is formed in an element active region on a semiconductor substrate, comprising:

a non-LOCOS insulating device isolation block formed by filling a first insulating film in a groove formed in said semiconductor substrate to demarcate said element active region on said semiconductor substrate;

a second insulating film covering said gate; and

a leading-out electrode filled, with intermediary of said second insulating film, between adjacent ones of said gates, having an upper surface which is planarized to be on substantially the same plane as that of an upper surface of said second insulating film, and connected to said source or drain.

69. A device according to claim 68, wherein said leading-out electrode is planarized by chemical mechanical polishing.

70. A device according to claim 68, wherein said gate is formed across said element active region and said first insulating film.

71. A device according to claim 68, wherein said leading-out electrode is planarized by chemical mechanical polishing.

72. A device according to claim 68, wherein said gate

and said leading-out electrode are formed of silicon films.

73. A device according to claim 68, further comprising a diffusion prevention film covering at least an inner wall surface of the groove, and wherein said first insulating film is filled in the groove with intermediary of said diffusion prevention film.

74. A device according to claim 68, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

75. A semiconductor device in which first and second transistors are stacked,

wherein said first transistor has a first gate patterned on a semiconductor substrate with intermediary of a first gate insulating film, and first source and drain formed in surface regions of said semiconductor substrate on both sides of said first gate,

an insulating interlayer having an upper surface is formed to cover said first gate, and

said second transistor includes a conductive film patterned on said insulating interlayer, and has a second gate patterned on said conductive film through a second gate insulating film and second source and drain formed in said conductive film on both sides of said second gate.

76. A device according to claim 75, wherein said insulating interlayer is planarized by chemical mechanical polishing.

77. A device according to claim 75, wherein said first source and said first drain have a conductivity type different from that of said second source and said second drain.

78. A device according to claim 75, wherein said first source and said first drain have the same conductivity type as that of said second source and said second drain.

79. A device according to claim 75, wherein said conductive film is formed of a silicon film.

80. A device according to claim 75, further comprising a silicide layer of a refractory metal formed on surfaces of said first and second gates.

81. A device according to claim 75, further comprising a step structure formed on said semiconductor substrate,

said step structure being formed in said insulating interlayer and planarized such that an upper surface of said step structure and an upper surface of said insulating interlayer are on substantially the same plane.

82. A device according to claim 81, wherein said insulating interlayer is planarized by chemical mechanical polishing.

83. A device according to claim 75, wherein a step structure is formed on said semiconductor substrate, an upper portion of another first gate is patterned on said step structure, and

said step structure and said another first gate are formed in said insulating interlayer and planarized such that an upper surface of said another first gate and said upper surface of said insulating interlayer are on substantially the same plane.

84. A device according to claim 83, wherein said insulating interlayer is planarized by chemical mechanical polishing.

85. A device according to claim 83, wherein said step

structure is a non-LOCOS insulating device isolation block for demarcating an element active region where said first transistor is formed on said semiconductor substrate.

86. A device according to claim 75, further comprising a first side wall formed on a side surface of said first gate of said first transistor, and

wherein each of said first source and drain is constituted by a first lightly doped diffusion layer formed in said semiconductor substrate near a lower portion of said first side wall, and a first heavily doped diffusion layer formed in said semiconductor substrate to be joined to said first lightly doped diffusion layer.

87. A device according to claim 75, further comprising a second side wall formed on a side surface of said second gate of said second transistor, and

wherein each of said second source and drain is constituted by a second lightly doped diffusion layer formed in said conductive film near a lower portion of said second side wall, and a second heavily doped diffusion layer formed in said conductive film to be joined to said second lightly doped diffusion layer.

88. A device according to claim 75, further comprising a cap insulating film formed on said first gate, and wherein said conductive film is formed on planarized surfaces of said insulating interlayer and said cap insulating film.

89. A semiconductor device comprising:

a semiconductor substrate;

an insulating film formed on said semiconductor substrate and having an opening for exposing a part of a surface of said semiconductor substrate;

a lower electrode patterned on said insulating film to bury the opening and having a planarized upper surface;

an upper electrode patterned on said lower electrode with intermediary of a dielectric film and capacitively coupled to said lower electrode,

wherein another insulating film is formed to bury sides of said lower electrode, said dielectric film and said upper electrode, said another insulating film being planarized to have a top surface flushed with the top surface of said upper electrode.

90. A device according to claim 89, wherein said upper surfaces of said lower electrode and said insulating film is planarized by chemical mechanical polishing.

91. A method of manufacturing a semiconductor device, comprising:

a first step for patterning a first insulating film on a reference layer;

a second step for forming step structure portions respectively on said first insulating film and said reference layer;

a third step for depositing a first conductive film on an entire surface of said reference layer including said step structure portions on said first insulating film to bury said step structure portions in said first conductive film;

a fourth step for polishing said first conductive film using said step structure portions on said first insulating film as stoppers until surfaces of said step structure portions on said first insulating film are exposed; and

a fifth step for patterning said first conductive film

to form a predetermined pattern consisting of said first conductive film on said reference layer and said step structure portions.

92. A method according to claim 91, wherein the fourth step includes polishing said first conductive film by chemical mechanical polishing.

93. A method according to claim 91, wherein said reference layer in the first step is a semiconductor substrate, and the first step includes forming said first insulating film on a scribing line region of said semiconductor substrate.

94. A method according to claim 91, wherein said step structure portions formed on said semiconductor substrate in the second step are non-LOCOS insulating device isolation blocks for demarcating an element active region.

95. A method according to claim 94, wherein said first conductive film in the third step is a polysilicon film, and

the fourth step includes forming a silicide layer of a refractory metal on said polished surface of said first conductive film and forming a polycide layer consisting of said first conductive film and said silicide layer.

96. A method according to claim 95, further comprising, between the second step and the third step, a sixth step for forming a second insulating film on said exposed semiconductor substrate, and

wherein the fourth step includes depositing a third insulating film on said silicide layer, and

the fifth step includes patterning said third insulating film and said polycide layer to form a predetermined pattern consisting of said polycide layer and

said third insulating film on said semiconductor substrate and said non-LOCOS insulating device isolation blocks, and

said method further comprises, after the fifth step, a seventh step for forming a fourth insulating film on a side surface of at least said polycide layer and removing said second insulating film on said semiconductor substrate between said pattern and said non-LOCOS insulating device isolation block.

97. A method according to claim 91, wherein said reference layer in the first step is an insulating interlayer deposited on a semiconductor substrate, and the second step includes forming said step structure portion from a patterned second conductive film and a second insulating film covering said second conductive film.

98. A method according to claim 97, wherein said first conductive film in the third step is a polysilicon film,

the fourth step includes forming a silicide layer of a refractory metal on said planarized surface of said first conductive film, and

the fifth step includes patterning said first conductive film together with said silicide layer to form a predetermined pattern consisting of said first conductive film and said silicide layer on said insulating interlayer and said step structure portions.

99. A method of manufacturing a semiconductor device, comprising:

a first step for forming a groove portion in a semiconductor substrate serving as a reference layer;

a second step for forming a step structure portion having a height smaller than a depth of the groove portion

on a bottom surface in the groove portion;

a third step for depositing a first conductive film on an entire surface of said semiconductor substrate including the groove portion to bury said step structure portion in said first conductive film;

a fourth step for polishing said first conductive film using said semiconductor substrate around the groove portion as a stopper until a surface of said semiconductor substrate is exposed; and

a fifth step for patterning said first conductive film to form a predetermined pattern of said first conductive film on said bottom surface in the groove portion and on said step structure portion.

100. A method according to claim 99, wherein the fourth step includes polishing said first conductive film by chemical mechanical polishing.

101. A method according to claim 100, wherein the step structure portion in the second step is an non-LOCOS insulating device isolation block for demarcating an element active region.

102. A method according to claim 100, wherein said first conductive film in the third step is a polysilicon film, and

the fourth step includes forming a silicide layer of a refractory metal on a polished surface of said first conductive film and forming a polycide layer consisting of said first conductive film and said silicide layer.

103. A method according to claim 102, wherein said method comprises, between the second step and the third step, a sixth step for forming a second insulating film on

said bottom surface in the exposed groove portion,

the third step includes depositing a third insulating film on said silicide layer,

the fifth step includes patterning said third insulating film and said polycide layer to form a predetermined pattern consisting of said polycide layer and said third insulating film on said semiconductor substrate and said non-LOCOS insulating device isolation block, and

said method further comprises, after the fifth step, a seventh step for forming a fourth insulating film on a side surface of at least said polycide layer and removing said second insulating film on said bottom surface between said pattern and said non-LOCOS insulating device isolation block.

104. A method of manufacturing a semiconductor device, comprising the steps of:

forming non-LOCOS insulating device isolation blocks in element isolation regions on a semiconductor substrate;

forming a first insulating film on a surface of said semiconductor substrate in an element formation region surrounded and demarcated by said non-LOCOS insulating device isolation blocks;

forming a first conductive film on an entire surface of said semiconductor substrate including said first insulating film to a thickness for burying said non-LOCOS insulating device isolation blocks;

polishing said first conductive film to leave said first conductive film having a predetermined thickness on said non-LOCOS insulating device isolation block and planarize a surface of said first conductive film;

forming a second insulating film on said planarized first conductive film;

patterning said second insulating film and said first conductive film to form patterns each consisting of said second insulating film and said first conductive film on said element formation region and said non-LOCOS insulating device isolation blocks;

forming a third insulating film on a side surface of at least said first conductive film of said pattern and removing said first insulating film between said patterns;

forming a second conductive film on an entire surface of said semiconductor substrate including a space between said patterns from which said first insulating film is removed to a thickness for burying the space between said patterns; and

polishing said second conductive film until said second insulating film of said pattern is exposed.

105. A method according to claim 104, wherein said first and second conductive films are polished by chemical mechanical polishing.

106. A method according to claim 104, further comprising a step for forming said third insulating film by performing anisotropic etching of an insulating film formed on said entire surface of said semiconductor substrate including the space between said patterns, and simultaneously removing said first insulating film between said patterns by the anisotropic etching.

107. A method according to claim 104, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

108. A method of manufacturing a semiconductor device, comprising the steps of:

forming non-LOCOS insulating device isolation blocks in element isolation regions on a semiconductor substrate;

forming a first insulating film on a surface of said semiconductor substrate in an element formation region surrounded and demarcated by said non-LOCOS insulating device isolation blocks;

forming a first conductive film on an entire surface of said semiconductor substrate including said first insulating film to a thickness for burying said non-LOCOS insulating device isolation blocks;

polishing said first conductive film to planarize a surface of said first conductive film using said non-LOCOS insulating device isolation blocks as stoppers;

forming a second conductive film on an entire surface of said semiconductor substrate including said non-LOCOS insulating device isolation blocks;

forming a second insulating film on said second conductive film;

patterning said second insulating film and said first and second conductive films to form patterns each consisting of said second insulating film and said first and second conductive films on said element formation region and said non-LOCOS insulating device isolation blocks;

forming a third insulating film on side surfaces of at least said first and second conductive films of said pattern and removing said first insulating film between said patterns;

forming a third conductive film on an entire surface of

said semiconductor substrate including a space between said patterns from which said first insulating film is removed, to a thickness to fill said space between said patterns; and

polishing said third conductive film until said second insulating film of said pattern is exposed.

109. A method according to claim 108, wherein said first and third conductive films are polished by chemical mechanical polishing.

110. A method according to claim 108, further comprising a step of forming said third insulating film by performing anisotropic etching of an insulating film formed on said entire surface of said semiconductor substrate including the space between said patterns and simultaneously removing said first insulating film between said patterns by the anisotropic etching.

111. A method according to claim 108, wherein said non-LOCOS insulating device isolation block is formed as a field shield element isolation structure.

112. A method according to claim 108, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

113. A method of manufacturing a semiconductor device having a transistor with a gate, a source, and a drain, comprising steps of:

covering said gate with an insulating film;

forming a conductive film constituting a part of a leading-out electrode of said source or drain to cover an upper portion of said insulating film; and

polishing said conductive film until said upper portion of said insulating film is exposed.

114. A method according to claim 113, wherein said conductive film is polished by chemical mechanical polishing.

115. A method according to claim 113, wherein said insulating film to be exposed in the step of polishing said conductive film is a gate cap insulating film.

116. A method of manufacturing a semiconductor device, comprising steps of:

forming a first insulating film on a surface of a semiconductor substrate in an element formation region surrounded and demarcated by non-LOCOS insulating device isolation blocks formed in element isolation regions on said semiconductor substrate;

forming a first conductive film on an entire surface of said semiconductor substrate including said first insulating film to a thickness for burying said non-LOCOS insulating device isolation blocks;

removing a part of said first conductive film to leave said first conductive film having a predetermined thickness on said non-LOCOS insulating device isolation block and planarize a surface of said first conductive film;

forming a second insulating film having an acid resistance on said planarized first conductive film;

forming a third insulating film on said second insulating film;

patterning said second and third insulating films and said first conductive film to form patterns each consisting of said second and third insulating films and said first conductive film on said element formation region and said non-LOCOS insulating device isolation blocks;

forming a fourth insulating film having an acid resistance on a side surface of at least said first conductive film of said pattern and removing said first insulating film between said patterns;

cleaning said third insulating film of said pattern to reduce a width of said third insulating film;

forming a second conductive film on an entire surface of said semiconductor substrate including a space between said patterns from which said first insulating film is removed, to a thickness to bury said patterns; and

polishing said second conductive film until said third insulating film of said pattern is exposed.

117. A method according to claim 116, wherein said first and second conductive films are polished by chemical mechanical polishing.

118. A method according to claim 116, further comprising steps of:

forming a fifth insulating film on said second conductive film and said third insulating film after polishing said second conductive film until said third insulating film of said pattern is exposed,

forming an opening in said fifth insulating film to expose part of a surface of said second conductive film, and

forming a third conductive film on said fifth insulating film to fill the opening.

119. A method according to claim 118, further comprising a step of using a polysilicon film for said second conductive film, and after polishing said second conductive film until said third insulating film of said pattern is

exposed and before forming at least said fifth insulating film, annealing said second conductive film to diffuse an impurity into said semiconductor substrate through said second conductive film to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on both sides of said pattern.

120. A method according to claim 116, further comprising, between forming said patterns each consisting of said second and third insulating films and said second conductive film and completion of cleaning at least said third insulating film, a step for removing said first insulating film between said patterns.

121. A method according to claim 116, further comprising a step for forming said third insulating film by plasma CVD.

122. A method according to claim 116, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

123. A method of manufacturing a semiconductor device, comprising the steps of:

forming a first insulating film on a surface of a semiconductor substrate in an element formation region surrounded and demarcated by non-LOCOS insulating device isolation blocks formed in element isolation regions on said semiconductor substrate;

forming a first conductive film on an entire surface of said semiconductor substrate including said first insulating film to a thickness for burying said non-LOCOS insulating device isolation blocks;

polishing said first conductive film using said non-

LOCOS insulating device isolation blocks as stoppers to planarize a surface of said first conductive film;

forming a second conductive film on an entire surface of said semiconductor substrate including said non-LOCOS insulating device isolation blocks;

forming a second insulating film having an acid resistance on said second conductive film;

forming a third insulating film on said second insulating film;

patterning said second and third insulating films and said first and second conductive films to form patterns each consisting of said second and third insulating films and said first and second conductive films on said element formation region and said non-LOCOS insulating device isolation blocks;

forming a fourth insulating film having an acid resistance on side surfaces of at least said first and second conductive films of said pattern and removing said first insulating film between said patterns;

cleaning said third insulating film of said pattern using an acid solution to reduce a width of said third insulating film;

forming a third conductive film on an entire surface of said semiconductor substrate including a space between said patterns from which said first insulating film is removed, to a thickness for burying said patterns; and

polishing said third conductive film until said third insulating film of said pattern is exposed.

124. A method according to claim 123, wherein said first and third conductive films are polished by chemical

mechanical polishing.

125. A method according to claim 124, further comprising steps of:

forming a fifth insulating film on said third conductive film and said third insulating film after polishing said third conductive film until said third insulating film of said pattern is exposed,

forming an opening in said fifth insulating film to expose part of a surface of said third conductive film, and

forming a fourth conductive film on said fifth insulating film to fill the opening.

126. A method according to claim 125, further comprising a step of using a polysilicon film for said third conductive film, and after polishing said third conductive film until said third insulating film of said pattern is exposed and before forming at least said fifth insulating film, annealing said third conductive film to diffuse an impurity into said semiconductor substrate through said third conductive film to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on both sides of said pattern.

127. A method according to claim 123, further comprising, between forming said patterns each consisting of said second and third insulating films and said first and second conductive films and completion of cleaning at least said third insulating film, a step for removing said first insulating film between said patterns.

128. A method according to claim 123, further comprising, immediately after cleaning said third insulating film of said pattern using the acid solution, a step for

annealing said third insulating film.

129. A method according to claim 123, further comprising a step for forming said third insulating film by plasma CVD.

130. A method according to claim 123, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

131. A method of manufacturing a semiconductor device, comprising:

a first step for patterning a first conductive film on a semiconductor substrate with intermediary of a first insulating film and forming said first insulating film to cover said first conductive film to bury said first conductive film in said first insulating film, thereby forming non-LOCOS insulating device isolation blocks on said semiconductor substrate to demarcate an element formation region;

a second step for forming a second insulating film on said semiconductor substrate in said element formation region;

a third step for filling a second conductive film, with intermediary of said second insulating film, between adjacent ones of said non-LOCOS insulating device isolation blocks on said semiconductor substrate;

a fourth step for sequentially depositing a third insulating film and a third conductive film on an entire surface of said non-LOCOS insulating device isolation blocks and said second conductive film; and

a fifth step for patterning said third conductive film, said third insulating film, said second conductive film,

and said second insulating film to form said third conductive film and said third insulating film into a strip shape and remove said second conductive film and said second insulating film between adjacent ones of said third conductive films.

132. A method according to claim 131, wherein the first step includes patterning said non-LOCOS insulating device isolation block into a strip shape, and

the fifth step includes pattering said third conductive film to be substantially perpendicular to said non-LOCOS insulating device isolation blocks.

133. A method according to claim 131, wherein the third step includes depositing said second conductive film on an entire surface of said non-LOCOS insulating device isolation blocks and said second insulating film, surface-polishing said second conductive film using said first insulating films of said non-LOCOS insulating device isolation blocks as stoppers to fill said second conductive film between said non-LOCOS insulating device isolation blocks.

134. A method according to claim 133, wherein the third step includes polishing said second conductive film by chemical mechanical polishing.

135. A method according to claim 131, wherein, said third conductive film in the fourth step is a polysilicon film, and the fourth step includes forming a silicide layer of a refractory metal on a surface of said third conductive film, and

the fifth step includes patterning said polycide layer, said third insulating film, said second conductive film,

and said second insulating film to form said polycide layer and said third insulating film into a strip shape and removing said second conductive film and said second insulating film between adjacent ones of said polycide layers.

136. A method according to claim 131, wherein the fourth step includes depositing a fourth insulating film on said third conductive film after formication of said third conductive film,

the fifth step includes patterning said fourth insulating film, said third conductive film, said second conductive film, and said second insulating film to form said fourth insulating film, said third conductive film, and said third insulating film into a strip shape,

said method further comprises, after the fifth step, a sixth step for forming a fifth insulating film on a side surface of at least said second conductive film, said third insulating film, and said third conductive film, and

a seventh step for filling a fourth conductive film between adjacent ones of said fifth insulating films on said semiconductor substrate.

137. A method according to claim 136, wherein the fourth step includes using a polysilicon film for said third conductive film, forming a silicide layer of a refractory metal on a surface of said third conductive film to form a polycide layer consisting of said third conductive film and said silicide layer, and forming said fourth insulating film on said polycide layer,

the fifth step includes patterning said fourth insulating film, said polycide layer, said third insulating

film, said second conductive film, and said second insulating film to form said polycide layer and said third insulating film into a strip shape and removing said second conductive film and said second insulating film between adjacent ones of said polycide layers, and

the sixth step includes forming said fifth insulating film on side surfaces of at least said second conductive film, said third insulating film, and said polycide layer.

138. A method according to claim 131, wherein the seventh step includes forming said fourth conductive film from undoped polysilicon, and

said method further comprises, after the seventh step, an eight step for doping an impurity in said fourth conductive film and diffusing the impurity into a surface region of said semiconductor substrate under said fourth conductive film to form an impurity diffusion layer.

139. A method according to claim 131, wherein the seventh step includes depositing said fourth conductive film on an entire surface of said semiconductor substrate including said fifth insulating film, surface-polishing said fourth conductive film using said fourth insulating film as a stopper, and filling said fourth conductive film between adjacent ones of said fifth insulating films.

140. A method according to claim 131, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

141. A method of manufacturing a semiconductor device, comprising steps of:

forming a first insulating film on a step structure nonformation region on a semiconductor substrate having a

step structure;

forming a first conductive film on an entire surface including said step structure;

polishing said first conductive film using an upper surface of said step structure as a stopper to planarize a surface of said first conductive film;

patterning said planarized first conductive film to leave said first conductive film into a predetermined shape in said nonformation region;

doping a first impurity in surface regions of said semiconductor substrate on both sides of said first conductive film to form a pair of first diffusion layers;

forming a second insulating film on an entire surface including said step structure and said first conductive film;

polishing said second insulating film using said upper surface of said first conductive film as a stopper to planarize a surface of said second insulating film;

thermally oxidizing said upper surface of said first conductive film to form a third insulating film;

patterning a second conductive film on said second insulating film including said third insulating film; and

doping a second impurity in said second conductive film on both sides of a predetermined portion to form a pair of second diffusion layers except said predetermined portion on said second conductive film positioned on said third insulating film.

142. A method according to claim 141, wherein said first conductive film and said second insulating film are polished by chemical mechanical polishing.

143. A method according to claim 141, wherein said first and second conductive films are formed of silicon films.

144. A method according to claim 141, wherein the first and second impurities are of conductivity types opposite to each other.

145. A method according to claim 141, wherein the first and second impurities have the same conductivity type.

146. A method according to claim 141, wherein said step structure is a non-LOCOS insulating device isolation block for demarcating an element active region where said first conductive film is formed on said semiconductor substrate.

147. A method according to claim 146, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a third conductive film patterned with intermediary of a fourth insulating film and a fifth insulating film covering said third conductive film.

148. A method according to claim 141, wherein a silicide layer is formed on said first conductive film, and a polycide layer is formed from said first conductive film and said silicide layer.

149. A method of manufacturing a semiconductor device, comprising steps of:

forming a first insulating film in a step structure nonformation region on a semiconductor substrate having a step structure;

forming first conductive film on an entire surface including said step structure;

polishing said first conductive film using an upper surface of said step structure as a stopper to planarize a surface of said first conductive film;

forming a second conductive film on said planarized first conductive film;

patterning said first and second conductive films into a predetermined shape to leave said first and second conductive films in said step structure nonformation region and leave only said second conductive film on said step structure;

doping a first impurity in surface regions of said semiconductor substrate on both sides of said first and second conductive films to form a pair of diffusion layers;

forming a second insulating film on an entire surface including said step structure and said second conductive film;

polishing said second insulating film using an upper surface of said second conductive film to planarize a surface of said second insulating film;

thermally oxidizing said upper surface of said second conductive film to form a third insulating film;

patterning a third conductive film on said second insulating film including said third insulating film; and

doping a second impurity in said third conductive film on both sides of a predetermined portion to form a pair of second diffusion layers except said predetermined portion on said third conductive film positioned above said third insulating film.

150. A method according to claim 149, wherein said first conductive film and said second insulating film are polished by chemical mechanical polishing.

151. A method according to claim 149, wherein said first to third conductive films are formed of silicon films.

152. A method according to claim 149, wherein the first and second impurities are of conductivity types opposite to each other.

153. A method according to claim 149, wherein the first and second impurities have the same conductivity type.

154. A method according to claim 149, wherein said step structure is a non-LOCOS insulating device isolation block for demarcating an element active region where said first and second conductive films are formed on said semiconductor substrate.

155. A method according to claim 154, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a fourth conductive film patterned with intermediary of a fourth insulating film and a fifth insulating film covering said fourth conductive film.

156. A method according to claim 149, wherein a silicide layer of a refractory metal is formed on said surface of said second conductive film.

157. A method of manufacturing a semiconductor device having a first transistor and a second transistor having a second source and a second drain, said first and second transistors having a common gate, comprising steps of:

patterning said gate on a semiconductor substrate with intermediary of a first gate insulating film and doping a first impurity in surface regions of said semiconductor substrate on both sides of said gate to form a first source and a first drain, for constituting said first transistor;

forming an insulating interlayer to cover said first transistor and polishing said insulating interlayer using

said gate as a stopper to planarize a surface of said insulating interlayer;

thermally oxidizing an exposed upper surface of said gate to form a second gate insulating film; and

patterning a conductive film on said insulating interlayer including said second gate insulating film and doping a second impurity in said conductive film while masking a portion of said conductive film positioned above said second gate insulating film to form said second source and said second drain, thereby constituting said second transistor.

158. A method according to claim 157, wherein said insulating interlayer is polished by chemical mechanical polishing.

159. A method according to claim 157, wherein said gate and said conductive film are formed of silicon films.

160. A method according to claim 157, wherein the first and second impurities are of conductivity types opposite to each other.

161. A method according to claim 157, wherein the first and second impurities have the same conductivity type.

162. A method of manufacturing a semiconductor device having a first transistor and a second transistor having a second source and a second drain, said first and second transistors having a common gate, comprising the steps of:

forming non-LOCOS insulating device isolation blocks for demarcating an element active region on a semiconductor substrate;

forming a first gate oxide film on a surface of said element active region;

forming a first conductive film on an entire surface including said non-LOCOS insulating device isolation blocks;

patterning said first conductive film to form said first conductive film into a predetermined shape in said element active region and to leave an upper portion of said first conductive film on said non-LOCOS insulating device isolation block, for forming said gate;

doping a first impurity in surface regions of said semiconductor substrate on both sides of said gate in said element active region to form a first source and a first drain, for constituting said first transistor;

forming an insulating interlayer to cover said first transistor and polishing said insulating interlayer using said gate as a stopper to planarize a surface of said insulating interlayer;

thermally oxidizing an exposed upper surface of said gate to form a second gate insulating film; and

patterning a second conductive film on said insulating interlayer including said second gate insulating film and doping a second impurity in said conductive film while masking a portion of said second conductive film positioned above said second gate insulating film to form said second source and said second drain, for constituting said second transistor.

163. A method according to claim 162, wherein said insulating interlayer is polished by chemical mechanical polishing.

164. A method according to claim 162, wherein said first and second conductive films are formed of silicon films.

165. A method according to claim 162, wherein the first

and second impurities are of conductivity types opposite to each other.

166. A method according to claim 162, wherein the first and second impurities have the same conductivity type.

167. A method according to claim 162, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a shield plate electrode patterned with intermediary of a shield gate insulating film and an insulating film covering said shield plate electrode.

168. A method according to claim 162, wherein a silicide layer of a refractory metal is formed on a surface of said gate.

169. A method according to claim 162, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

170. A method of manufacturing a semiconductor device comprising:

a first step for sequentially forming a first insulating film and a first conductive film on a semiconductor substrate;

a second step for patterning said first conductive film, said first insulating film, and said semiconductor substrate to form a groove from said first conductive film to a predetermined depth of said semiconductor substrate;

a third step for forming a second insulating film on an entire surface to cover an inner wall of the groove;

a fourth step for forming a third insulating film on an entire surface including the groove;

a fifth step for polishing said third insulating film

to planarize said third insulating film until said first conductive film is exposed and filling said third insulating film in the groove;

a sixth step for sequentially forming a second conductive film and a fourth insulating film on an entire surface including said planarized third insulating film;

a seventh step for patterning said fourth insulating film, said second conductive film, said first conductive film, and said first insulating film to form a pattern consisting of said first insulating film, said first conductive film, said second conductive film, and said fourth insulating film into a predetermined shape in at least a groove nonformation region on said semiconductor substrate;

an eighth step for forming a fifth insulating film on side surfaces of at least said first and second conductive films;

a ninth step for forming a third conductive film on an entire surface including a space between said first and second conductive films adjacent to each other with intermediary of said fifth insulating film; and

a tenth step for polishing said third conductive film to planarize said third conductive film until said fourth insulating film is exposed and filling said third conductive film, with intermediary of said fifth insulating film, between said first and second conductive films adjacent to each other.

171. A method according to claim 170, wherein said third insulating film and said third conductive film are polished by chemical mechanical polishing.

172. A method according to claim 170, wherein said third insulating film in the groove is an non-LOCOS insulating device isolation block for demarcating an element active region on said semiconductor substrate.

173. A method according to claim 170, wherein said first to third conductive films are formed of silicon films.

174. A method according to claim 170, wherein the seventh step includes, when said fourth insulating film, said second conductive film, said first conductive film, and said first insulating film are to be patterned to form said pattern, leaving said fourth insulating film and said second conductive film on said third insulating film to form said pattern across said nonformation region and said third insulating film.

175. A method of manufacturing a semiconductor device comprising:

a first step for forming a first gate insulating film on a surface of a semiconductor substrate;

a second step for patterning a first gate on said first gate insulating film;

a third step for doping a first impurity in surface regions of said semiconductor substrate on both sides of said first gate to form a pair of first impurity diffusion layers;

a fourth step for forming an insulating interlayer to cover said first gate and polishing said insulating interlayer to planarize a surface of said insulating interlayer;

a fifth step for patterning a conductive film on said insulating interlayer;

a sixth step for forming a second gate insulating film on a surface of said conductive film;

a seventh step for patterning a second gate on said second gate insulating film; and

an eighth step for doping a second impurity in surface regions of said conductive film on both sides of said second gate to form a pair of second impurity diffusion layers.

176. A method according to claim 175, wherein said first and second gates and said conductive film are formed of silicon films.

177. A method according to claim 175, wherein the first and second impurities are of conductivity types opposite to each other.

178. A method according to claim 175, wherein the first and second impurities have the same conductivity type.

179. A method according to claim 175, wherein the second step includes pattering a cap insulating film on said first gate together with said first gate.

180. A method according to claim 175, wherein the third step includes lightly doping the first impurity in said semiconductor substrate to form said first impurity diffusion layers as first lightly doped diffusion layers, and

further comprising, between the third step and the fourth step, a ninth step for forming a first side wall on a side surface of said first gate, and

a tenth step for heavily doping said semiconductor substrate on both sides of said first side wall with said first impurity to form first heavily doped diffusion layers joined to said first lightly doped diffusion layers.

181. A method according to claim 175, wherein the eighth step includes lightly doping the second impurity in said conductive film to form said second impurity diffusion layers as second lightly doped diffusion layers, and

further comprising, after the eighth step, an eleventh step for forming a second side wall on a side surface of said second gate, and

a twelfth step of heavily doping the second impurity in said conductive film on both sides of said second side wall to form second heavily doped diffusion layers joined to said second lightly doped diffusion layers.

182. A method of manufacturing a semiconductor device, comprising:

a first step for forming non-LOCOS insulating device isolation blocks for demarcating an element active region on a semiconductor substrate;

a second step for forming a first gate insulating film on a surface of said element active region;

a third step for forming a first conductive film on an entre surface including said non-LOCOS insulating device isolation blocks;

a fourth step for patterning said first conductive film to form said first conductive film into a predetermined shape in said element active region with intermediary of said first gate insulating film and leave an upper portion of said first conductive film on said non-LOCOS insulating device isolation block, for forming a first gate;

a fifth step for doping a first impurity in surface regions of said semiconductor substrate on both sides of said first gate in said element active region to form a pair

of first impurity diffusion layers;

a sixth step for forming an insulating interlayer to cover said first gate and polishing said insulating interlayer to planarize a surface of said insulating interlayer;

a seventh step for pattering a second conductive film on said insulating interlayer including said second gate insulating film;

an eighth step for forming a second gate insulating film on a surface of said second conductive film;

a ninth step for forming a third conductive film on said second gate insulating film and patterning said third conductive film to form a second gate; and

a tenth step for doping a second impurity in surface regions of said conductive film on both sides of said second gate to form a pair of second impurity diffusion layers.

183. A method according to claim 182, wherein said insulating interlayer is polished by chemical mechanical polishing.

184. A method according to claim 182, wherein said first to third conductive films are formed of silicon films.

185. A method according to claim 182, wherein the first and second impurities are of conductivity types opposite to each other.

186. A method according to claim 182, wherein the first and second impurities have the same conductivity type.

187. A method according to claim 182, wherein said non-LOCOS insulating device isolation block is a field shield element isolation structure having a shield plate electrode patterned with intermediary of a shield gate insulating

film and an insulating film covering said shield plate electrode.

188. A method according to claim 182, wherein a silicide layer of a refractory metal is formed on a surface of said gate.

189. A method according to claim 182, wherein the fourth step includes pattering a cap insulating film on said first gate together with said first gate.

190. A method according to claim 182, wherein the fifth step includes lightly doping the first impurity in said semiconductor substrate to form said first impurity diffusion layers, and

further comprising, between the fifth step and the sixth step, an eleventh step of forming a first side wall on a side surface of said first gate, and

a twelfth step of heavily doping said semiconductor substrate on both sides of said first heavily doped diffusion layers first impurity to form first lightly doped diffusion layers.

191. A method according to claim 182, wherein the tenth step includes lightly doping the second impurity in said conductive film to form said second impurity diffusion layers as second lightly doped diffusion layers, and

further comprising, after the tenth step, a thirteenth step for forming a second side wall on a side surface of said second gate, and

a fourteenth step for heavily doping said conductive film on both sides of said second side wall with said second impurity to form second heavily doped diffusion layers

joined to said second lightly doped diffusion layers.

192. A method according to claim 182, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

193. A method of manufacturing a semiconductor device comprising steps of:

forming an insulating film on a semiconductor substrate;

forming an opening in said insulating film to expose a part of a surface of said semiconductor substrate;

forming a first conductive film on said insulating film to fill the opening;

polishing a surface of said first conductive film to planarize said first conductive film;

sequentially forming a dielectric film and a second conductive film on said planarized first conductive film;

simultaneously patterning said second conductive film, said dielectric film, and said first conductive film into a capacitor shape;

forming an insulating film to cover said second conductive film, said dielectric film and said first conductive film, respectively patterned into the capacitor shape; and

polishing said insulating film using said second conductive film as a stopper to planarizi, until the surface of said second conductive film is exposed.

194. A method according to claim 193, wherein said surface of said first conductive film and said insulating film are polished by chemical mechanical polishing.

195. A method of manufacturing a semiconductor device,

comprising steps of:

forming non-LOCOS insulating device isolation blocks in an element isolation region on a semiconductor substrate;

forming a first insulating film on a surface of said semiconductor substrate in an element formation region surrounded and demarcated by said non-LOCOS insulating device isolation blocks;

forming a first conductive film on an entire surface of said semiconductor substrate including said first insulating film to a thickness to bury said non-LOCOS insulating device isolation blocks;

polishing said first conductive film using said non-LOCOS insulating device isolation blocks as stoppers to planarize a surface of said first conductive film;

forming an underlayer consisting of a refractory metal on an entire surface of said semiconductor substrate including said non-LOCOS insulating device isolation blocks;

forming a silicide film on said underlayer;

forming a second insulating film on said silicide film; and

patterning said second insulating film, said silicide film, said underlayer, and said first conductive film to form a pattern consisting of said first conductive film, said underlayer, said silicide film, and said second insulating film on said element formation region and said non-LOCOS insulating device isolation blocks.

196. A method according to claim 195, further comprising steps of:

forming a third insulating film on side surfaces of at least said first conductive film, said underlayer, and said

silicide film and removing said first insulating film between said patterns,

forming a second conductive film on an entire surface of said semiconductor substrate including a space between said patterns from which said first insulating film is removed to a thickness to fill the space between said patterns, and

polishing said second conductive film until said second insulating film of said pattern is exposed.

197. A method according to claim 195, wherein said underlayer is a titanium nitride film.

198. A method according to claim 195, wherein said silicide film is a tungsten silicide film.

199. A method according to claim 195, wherein said first conductive film is polished and planarized by chemical mechanical polishing.

200. A method according to claim 196, wherein said second conductive film is polished and planarized by chemical mechanical polishing.

201. A method according to claim 195, wherein said non-LOCOS insulating device isolation block is a trench type element isolation structure.

202. A method of deleting information from a semiconductor device in use of said semiconductor device comprising non-LOCOS insulating device isolation blocks for demarcating element active regions on a semiconductor substrate, wherein said device comprises,

a first conductive film buried in a first insulating film;

a second conductive film formed into an island shape in

said element active region and filled with intermediary of second insulating films, in the region between said non-LOCOS insulating device isolation blocks in said element active region between adjacent ones of said non-LOCOS insulating device isolation blocks; and

a third conductive film formed on said second conductive film to oppose the second conductive film with intermediary of a third insulating film,

wherein said second conductive film is capacitively coupled to said third conductive film through said third insulating film, and capacitively coupled to said first conductive film through a side surface portion of said first insulating film:

the method comprising a step of applying a first voltage having a negative value to said first conductive film and a second voltage higher than the first voltage to said third conductive film to accumulate predetermined charges in said second conductive film, to shift a threshold value viewed from said third conductive film in a positive direction for deleting information.

203. A semiconductor device having a transistor with a gate, a source, and a drain formed in an element active region demarcated by element isolation structures on a semiconductor substrate, comprising:

at least two gate structures each including said gate covered with insulating film and formed on said element active region to extend over said element isolation structures; and

a leading-out electrode filled between adjacent ones of said gate structures,

wherein upper surfaces of said gate structures are planarized at substantially the same level over said element isolation structures and said element active region, and upper surfaces of said insulating films and an upper surface of said leading-out electrode are planarized at substantially the same level.

204. A device according to claim 203, wherein said upper surfaces of said gates, said upper surfaces of said insulating films, and said upper surface of said leading-out electrode are planarized by chemical mechanical polishing.

205. A device according to claim 203, wherein said element isolation structure is a field shield element isolation structure which has a shield plate electrode patterned with intermediary of a shield gate insulating film and a cap insulating film covering said shield plate electrode and fixes a portion of said semiconductor substrate positioned below said shield plate electrode to a predetermined potential.

206. A device according to claim 203, wherein upper surfaces of cap insulating films formed on said gates and the upper surface of said leading-out electrode are planarized at substantially the same level.

207. A device according to claim 203, wherein said element isolation structure is a trench type element isolation structure.

208. A semiconductor device comprising:

a first step structure portion made of a silicon film formed at a predetermined level from a surface of a semiconductor substrate;

a second step structure portions respectively formed on said first step structure portion and on said semiconductor substrate, said second step structure portion on said semiconductor substrate serving as a field oxide film for demarcating element active regions; and

conductive films patterned in said element active region to span over at least said second step structure portion on said semiconductor substrate,

wherein upper surfaces of said conductive films are planarized at substantially the same level.

209. A device according to claim 208, wherein said upper surfaces of said conductive films are planarized by a chemical mechanical polishing process.

210. A device according to claim 208, wherein each of said conductive films constitutes an element of gate structure of a transistor.

211. A device according to claim 208, wherein said first step structure portion is formed on a scribing line region of said semiconductor substrate.

212. A method of manufacturing a semiconductor device comprising:

a first step for patterning a silicon film on a semiconductor substrate;

a second step for applying field oxidation on said silicon film and said semiconductor substrate to form a field oxide film;

a third step for depositing a conductive film on entire surface of said semiconductor substrate including said field oxide film on said silicon film, to bury said field oxide film within said conductive film;

a fourth step for polishing said conductive film with using said field oxide film on said silicon film as a stopper until the surface of the field oxide film is exposed; and

a fifth step for patterning said conductive film to form a predetermined pattern of said conductive film on said semiconductor substrate and on said field oxide film formed on said semiconductor substrate.

213. A method according to claim 212, wherein said conductive film is polished by a chemical mechanical polishing process in said fourth step.

214. A method according to claim 212, wherein said silicon film is formed on a scribing line region on the semiconductor substrate in said first step.